System-Level I/O Power Modeling

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ABSTRACT

A methodology is proposed for the electrical characterization of electronic packages in a system-level environment. Modeling and simulation results show the capability of the method by demonstrating both power delivery and I/O signal integrity analysis in a unified environment. In addition to flexibility, the proposed method is capable of achieving accurate results in a fraction of the time as was previously required.

1. INTRODUCTION

The two major factors which dictate design tradeoffs from a performance perspective are I/O signal integrity and power delivery. I/O signal integrity relates to how the design of the package affects signal propagation. Ideally, signal lines are designed to behave very much like ideal transmission-lines. That is, discontinuities and changes in reference are minimized. However design tradeoffs often relax this requirement so that other performance metrics may be achieved. Compromises in I/O performance are usually at the expense of an improved power delivery solution, and vice versa. Power delivery relates to how well power can be delivered to the IC. The main goal in achieving an effective power delivery solution minimizes the voltage fluctuations on the die due the parasitic inductance and resistance of decoupling capacitors, packages, and boards.

Previously, package design metrics based upon I/O and power delivery performance were developed independently. This is becoming increasing inadequate due to the coupling between the I/O and power delivery networks. Metrics such as SSO pushout and power/ground fluctuations due to I/O switching serve to quantify the amount of coupling. However, quantifying such effects places an extreme burden upon the capability of current modeling and simulation software. It is not appropriate to separately model sections of the package or system. Proper characterization of the true coupling between power and I/O requires a solution which is capable of adequately resolving layout details while maintaining an acceptable level of engineering accuracy.

2. METHODOLOGY

Proper characterization of package performance requires the use of a method which is capable of accurately predicting the electromagnetic interactions at the board and package level. Models involving lumped circuit elements are being replaced with higher bandwidth, more distributed models. Full-wave models based upon solving an integral or differential equation in three-dimensional space are the ideal solution, however constraints placed upon computational resources renders such methods inadequate. What is needed is a hybrid or hierarchical approach capable of resolving full-wave effects for sections of the structure comparable to a wavelength, transmission-line effects for sections which exhibit such behavior, and finally lumped circuit perturbations for parasitics which do not require a full-wave description and do not behave like a transmission-line.

One approach involves modeling the power and ground planes as a distributed network of transmission-lines which are in turn coupled to the transmission-lines representing the I/O lines¹. In addition to being very tedious to implement, limitations placed upon the arrangement of the power and ground planes render this approach less than ideal for most practical applications. Other methods in use today are similar in concept, but vary in the manner in which the planes are modeled. For example, instead of modeling the plane pairs as transmission-lines, each section in the distributed network may be modeled using equivalent lumped elements. The same considerations apply with regard to the complexity of the model creation process. A model representing the package alone may easily require weeks to months to construct. This limitation renders the approach of manually modeling sections of the power/ground structure inadequate if short design cycle times are required.

Recently, a very promising solution has been proposed²⁻³. This approach takes advantage of the natural decoupling between the transmission-line and parallel plate waveguide modes. The solution process is a hierarchical one in that the parallel plate waveguide modes are solved for in a full-wave sense, the transmission-line modes are solved via telegrapher's equations by way of SPICE, and electrically small sections are represented by lumped equivalent elements in SPICE. The

solutions are coupled by a leap-frog in time process whereby vias (represented as lumped elements) connected to the transmission-lines couple current and therefore serve as the excitation for the parallel plate modes. The parallel plate mode solution adjusts the via current through the solution of Maxwell's equation between each plane layer, thus predicting the actual coupling between vias. After solving for the fields between the planes, the via current values are updated and fed back into the circuit solver. This process continues for each integral multiple of the time-step, as defined by Courant's stability requirement in the finite-difference time-domain solution. The efficiency of the overall solution is improved by eliminating the electric field components transverse to the z-direction (direction along which the board/package stackup is defined). In effect, the three-dimensional problem is reduced to a two-dimensional one in which the transverse magnetic and longitudinal or z-directed electric fields are solved.

3. RESULTS

When considering the impact of package design on package- or system-level metrics, it is often necessary to include the entire package and/or board to properly estimate signal integrity. Previously, the modeling and simulation of even a quadrant of a package required hours and sometimes days to complete. With this methodology, an entire system can be modeled and simulated in a matter of minutes to at most a couple of hours.

Consider the package whose top layer of four total layers is shown in Figure 1. For simplicity, only ten traces (shown in yellow) are considered. However, computation time does not significantly increase as more traces are added. Drivers are attached to each trace in the center region of the package. The drivers are modeled using a behavioral representation with voltage controlled resistor sources in SPICE. Power and ground to these drivers are provided by nearby VCC/VSS vias shown in red and blue, respectively.

Figure 1. Top layer of package.

Figure 2. Bottom layer of package.

Figure 2 shows an illustration of the bottom layer of the package with a projection of the top layer traces shown in gray. Power and ground is supplied to this package the VCC and VSS vias shown in red and blue, respectively. In this study, it is assumed that the generator is connected directed across the vias on this layer. The signal traces are routed on the top layer and transition to the bottom layer through via connections along the periphery of the package. Figure 2 shows these vias in yellow. Two $1\mu\text{F}$ decoupling capacitors are connected to the bottom layer of the package directly under the center VCC/VSS vias shown in Figure 2. These capacitors reduce the power and ground supply oscillation when multiple outputs are switching.

Figure 3 depicts the condition where all ten drivers are active. The dashed and dotted pulse waveforms illustrate the propagation along trace 5 (see Figure 1) at the driver and receiver positions, respectively. The waveform oscillating about 1.32V shows the variation in the supply voltage to the driver. Figure 4 shows the same waveforms as in Figure 3, except that only one driver is active in this case. By comparing both figures, the effect of multiple drivers driving simultaneously can be seen through the variation in the supply voltage.

Figure 3. Signal waveforms when 10 drivers are active.

Figure 4. Signal waveforms when 1 active is active.

The phenomenon called SSO pushout is a result of the multiple drivers switching simultaneously. It impacts signal integrity through adding an extra delay to the propagating signal. Previously, this was difficult or impossible to predict. System designers simply added in a few hundred nanoseconds to the timing budget to account for this degradation to the signal. Using the methodology described in this paper, measuring SSO pushout is as simple as measuring the difference between the receiver waveforms in Figures 3 and 4. As shown in Figure 5, the SSO pushout observed on trace 5 is 7ps. This may seem like a negligible effect, but when the package is attached to a board, then another package, the overall pushout suddenly becomes significant. Additionally, this example uses a 1ns risetime. High performance designs today may be well below 100ps. In that case, SSO pushout may become a very significant factor in the overall timing budget.

Figure 5. SSO pushout observed on trace 5.

4. REFERENCES

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